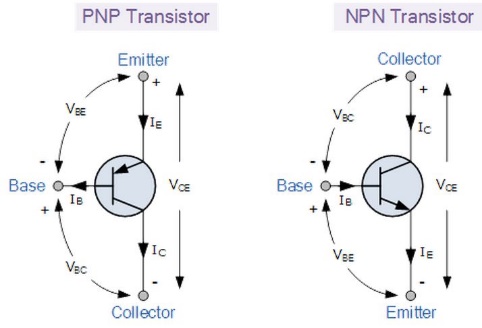
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| **SINGLE/MULTI STAGE AMPLIFIERS 설계** |
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**What is Amplifier ?**

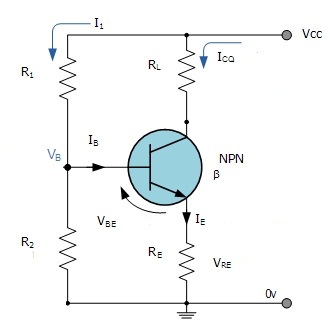
It is an electronic device that increases the power of a signal. It does this by taking energy from a power supply and controlling the output to match the input signal shape but with a larger amplitude.

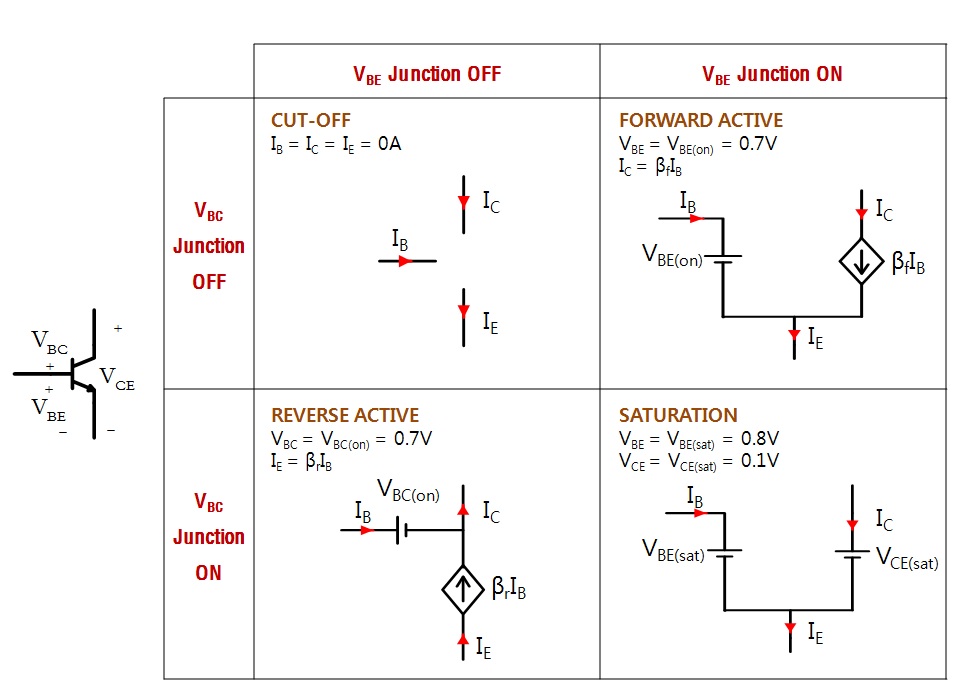
**Types of Bipolar Transistors**



* The Bipolar Junction Transistor (BJT) is a three layers device constructed form two semiconductor diode junctions joined together, one forward biased and one reverse biased.
* There are two main types of bipolar junction transistors, the NPN and the PNP transistor.
* Transistors are “**Current Operated Devices**” where a much smaller Base current causes a larger Emitter to Collector current, which themselves are nearly equal, to flow.
* The arrow in a transistor symbol represents conventional current flow.
* Requires a Biasing voltage for AC amplifier operation.
* The Base-Emitter junction is always forward biased whereas the Collector-Base junction is always reverse biased.
* The standard equation for currents flowing in a transistor is given as:  IE = IB + IC
* The Collector or output characteristics curves can be used to find either Ib, Ic or β to which a load line can be constructed to determine a suitable operating point, Q with variations in base current determining the operating range.
* A transistor can also be used as an electronic switch between its saturation and cut-off regions to control devices such as lamps, motors and solenoids etc..
* The NPN transistor requires the Base to be more positive than the Emitter while the PNP type requires that the Emitter is more positive than the Base.

**Bias Conditions for BJT**

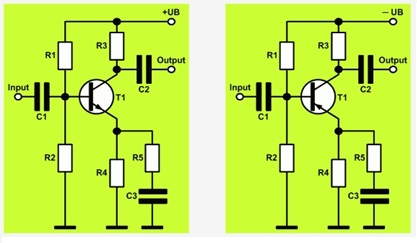




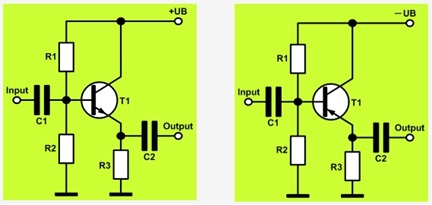
**Types of Amplifiers**

* The most common transistor connection is the Common Emitter (CE) configuration but Common Base (CB) and Common Collector (CC) are also available.

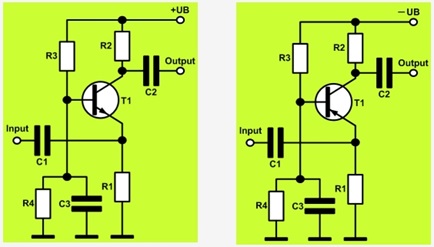
Common Emitter Amplifiers



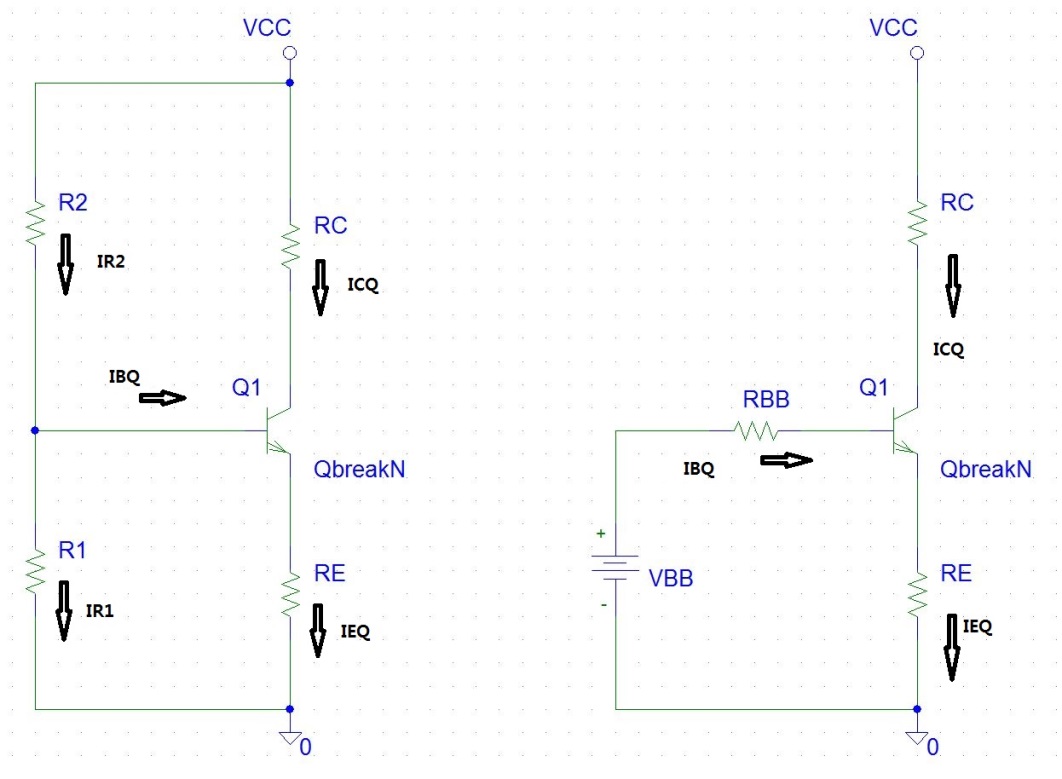
Common Base Amplifiers



Common Collector Amplifiers (Emitter Follower)



**Voltage Divider Bias Circuit for BJT Amplifiers**



The voltage divider is formed using external resistors R1 and R2. The voltage across R1 forward biases the emitter junction. By proper selection of resistors R1 and R2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor. The voltage divider configuration achieves the correct voltages by the use of resistors in certain patterns. By manipulating the resistors in certain ways you can achieve more stable current levels without having β value affect it too much.

We first analyze the bias circuit under DC conditions. The Thevenin equivalent voltage and resistance from base to ground are

For R2

For R1

Writing KVL equations around base loop, we obtain

and at the quiescent point,

We neglect VBE since we are dealing only time-varying components. The current restriction then becomes

Generally, RBB is to be set

This prevents variation in β from significantly affecting the dc operating point of the stage. The above equations are used in the design process.

**Merits:**

* Unlike above circuits, only one dc supply is necessary.
* Operating point is almost independent of β variation.
* Operating point stabilized against shift in temperature.

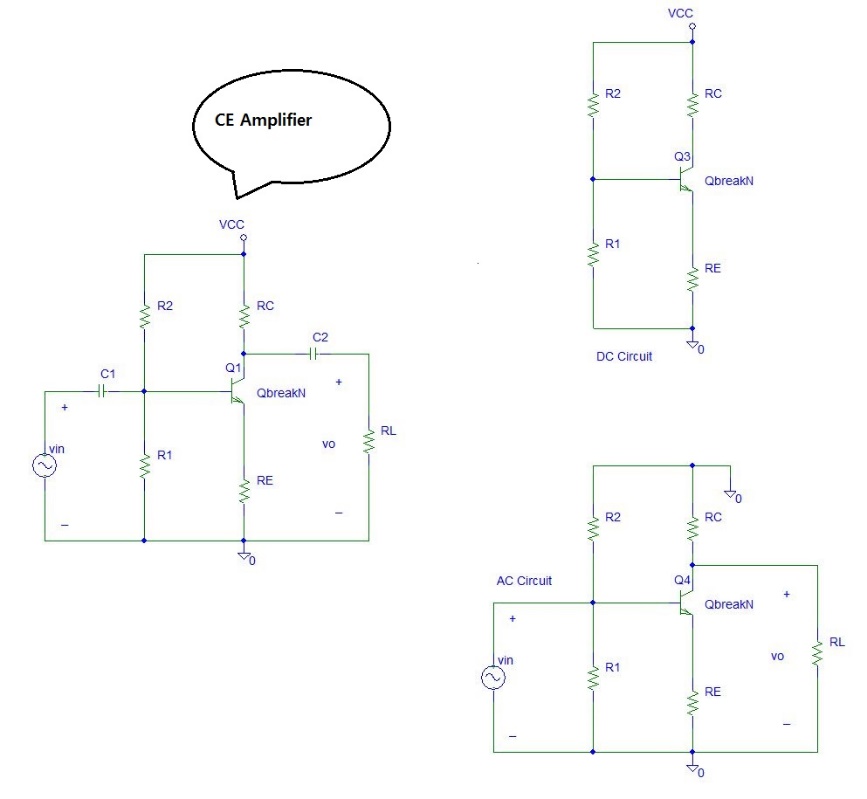
**Demerits:**

* As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE fairly large, or making R1||R2 very low.
  + If RE is of large value, high VCC is necessary. This increases cost as well as precautions necessary while handling.
  + If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R2 raises VB closer to VC, reducing the available swing in collector voltage, and limiting how large RC can be made without driving the transistor out of active mode. A low R1 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
* The standard voltage divider circuit discussed above faces a drawback – AC feedback caused by resistor RE reduces the gain. This can be avoided by placing a capacitor (CE) in parallel with RE, as shown in circuit diagram. The result is that the DC operating point is well controlled, while the AC-gain is much higher (approaching β), rather than the much lower (but predictable) value of R c / R e {\displaystyle R\_{\text{c}}/R\_{\text{e}}} without the capacitor.

**Usage:**

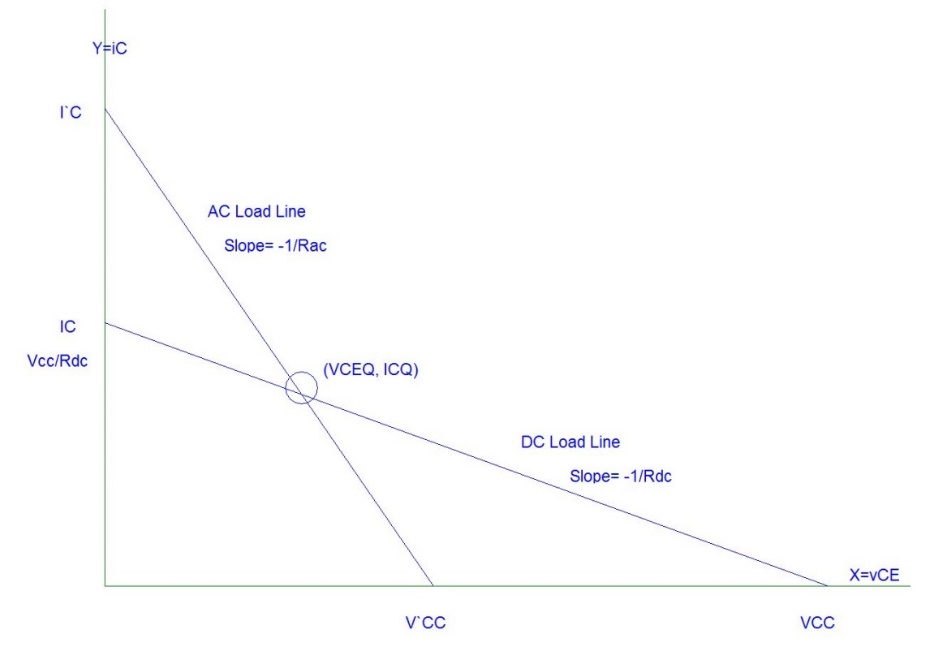
The circuit's stability and merits as above make it widely used for linear circuits.

**How to find Q-point for maximum output swing using AC and DC Load Lines**



DC circuit

AC circuit



Q-point of transistor for maximum output swing

Equation of DC Load Line

Equation of AC Load Line

Maximum collector current on AC load line

Bias voltage condition for maximum output swing

For VCEQ use AC and DC load lines

Bias current condition for maximum output swing

**Analysis of CE Amplifier**

Input resistance ;

Current gain ;

Voltage gain ;

**Design Procedure of CE Amplifier**

Step 1. Determine the value of RC using table

|  |  |  |  |
| --- | --- | --- | --- |
|  | Bias Current | Current Gain | vo(p-p) |
| RC = 1•RL | Medium | Medium | Medium |
| RC = 0.1•RL | High | Low | High |
| RC = 10•RL | Low | High | Low |

Step 2. Find Rdc and Rac

Step 3. Calculate the quiescent collector current, ICQ, needed to place the Q-point in the center of the AC load line(i.e. Maximum swing)

Step 4. Determine R`E using the voltage gain specification.

Step 5. Find small signal emitter resistance, re, and RE.

Step 6. If there are a current gain or input resistance specification for the design, we shall use it to solve for the value of bias resistance RBB. If not, we use the bias stability condition.

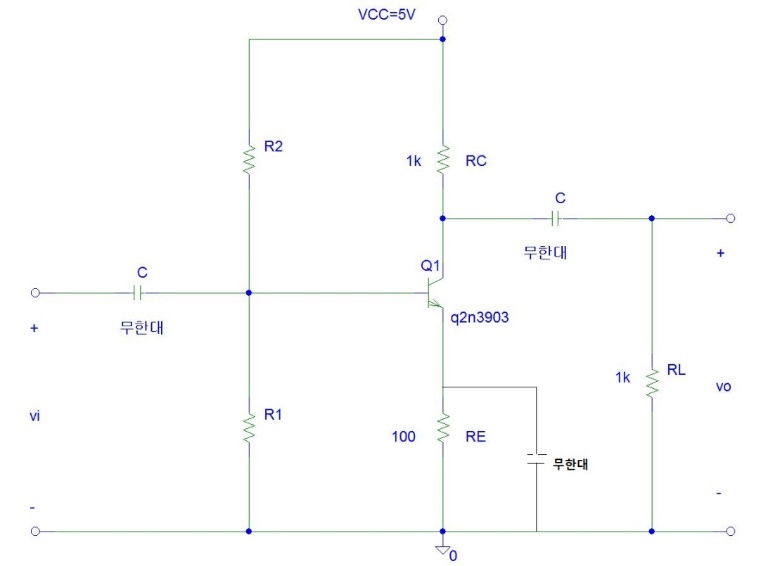
Step 7. Calculate the quiescent collector-emitter voltage, VCEQ.

Step 8. Calculate the quiescent base voltage, VBB.

Step 9. Calculate bias resistors R1 and R2.

**Design of Bias Circuit**

Example: Select R1 and R2 for maximum output voltage swing in the circuit shown in the below figure.



SOLUTION: We first determine ICQ for the circuit.

*Rac= RC∥RL = 500 Ω*

*Rdc = RE + RC =1100 Ω*

For maximum swing,¡

*V`CC = 2•VCEQ*

*VCEQ = ICQ•Rac = (3.13 mA)(500Ω) =1.56 V*

*V`CC = 2•VCEQ = 3.13 V*

From the manufacturer`s specification, the maximum β for the 2N3903 is 200. RB is set equal to 0.1(β)(RE) for bias stability,

*RBB = 0.1(200)(100) = 2 kΩ*

Since we know VBB and RBB, we find R1 and R2

:

The maximum output voltage swing, ignoring the nonlinearities at saturation and cutoff, would then be

*Maximum output swing= 2•ICQ•( RC∥RL) = 2(3.13mA)(500Ω)=3.13 V*

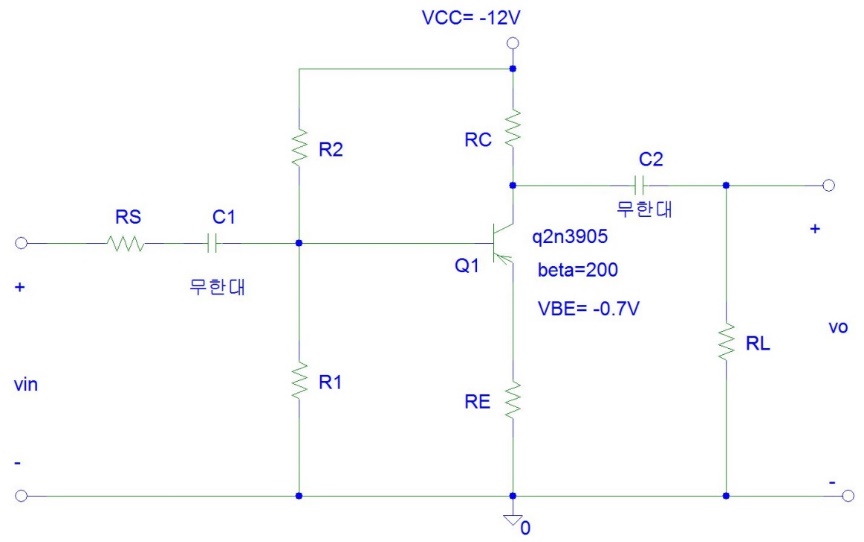
We check the maximum power dissipated by the transistor to assure that it will not exceed the specifications.

*P(transistor)= VCEQ•ICQ = (1.56 V)•(3.13 mA) = 4.87 mW*

This is well within the 350 mW maximum given on the specification.

**Capacitor-Coupled CE Amplifier Design**

Design a CE amplifier with Av=-10, β=200, and RL=1 kΩ. A *pnp* transistor is used and maximum symmetrical output swing is required. Check the value of Av using a computer simulation.



SOLUTION :

We shall choose RC = RL = 1 kΩ

Using the equation for Av to solve for RE,

When known values are substituted into this equation, we find R`E=50 Ω.

We need to know the value of re in order to find RE. We first find Rac and Rdc.

*Rac = RE + (RC∥RL) = 550 Ω*

*Rdc = RE + RC = 1050 Ω*

With Rac and Rdc determined, the design of this circuit now parallels the step-by-step procedure for the design. The first step is to calculate the quiescent current needed to place the Q-point in the center of the ac load line. The equation is

The quantity re is found as follows

Then

*RE = 50 – re = 46.5 Ω*

If there were a current gain or input resistance specification for this design, we would use it to solve for the value of RBB. Since there is no such specification, we use the expression

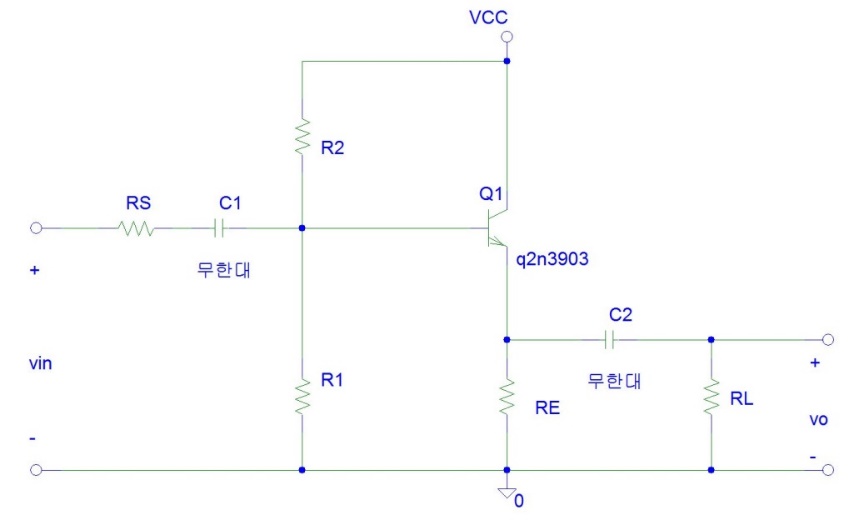
*RBB = 0.1βRE = 0.1(200)(46.5) = 930 Ω*

Then continuing with the design steps,

The maximum peak-to-peak output swing is given by

The power delivered into the load is given by

**Analysis of CC(Emitter Follower) Amplifier**



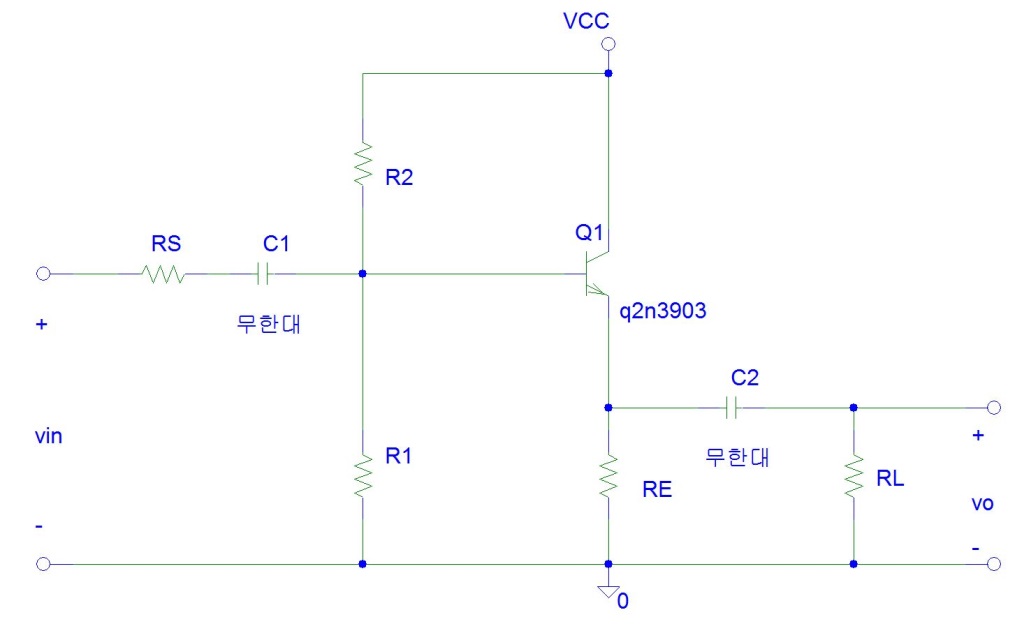
Input resistance ;

Current gain ;

Voltage gain ;

**Design of Capacitor-Coupled EF Amplifier**

Design a single-stage npn Emitter Follower amplifier with β=60, VBE=0.7 V, Rin= 1 kΩ, and VCC= 12 V. Determine the circuit element values for the stage to achieve A*i* =10 with a 100 Ω load.



**SOLUTION** We must select R1, R2, and RE but we have only two equations. These two equations are specified by the current gain and the placement of the Q-point. Previous example showed that the best choice for a CE amplifier is to make RC=RE. We could derive a similar result for RE and RL in the CC amplifier. We shall therefore begin by constraining RE to be equal to RL. This yield a third equation,

*RE=RL= 100 Ω*

Now finding the load line slopes,

*Rac = RL∥RE = 100 Ω*

*Rdc = RE = 100 Ω*

Since the amplitude of the input is not specified, we choose the quiescent current to place the Q-point in the center of the ac load line for maximum swing.

We now find the value of re

Since re is insignificant compared to RE∥RL, it can be ignored, which is usually the case for EF circuits.

Using the equation for the current gain, we find

Everything in this equation is known except RBB. We solve for RB**B** with the result

*RBB =1500 Ω*

VBB is found from the base loop.

Continuing with the design as presented earlier, we find

*R1= 13.5 kΩ*

and

*R2= 1.68 kΩ*

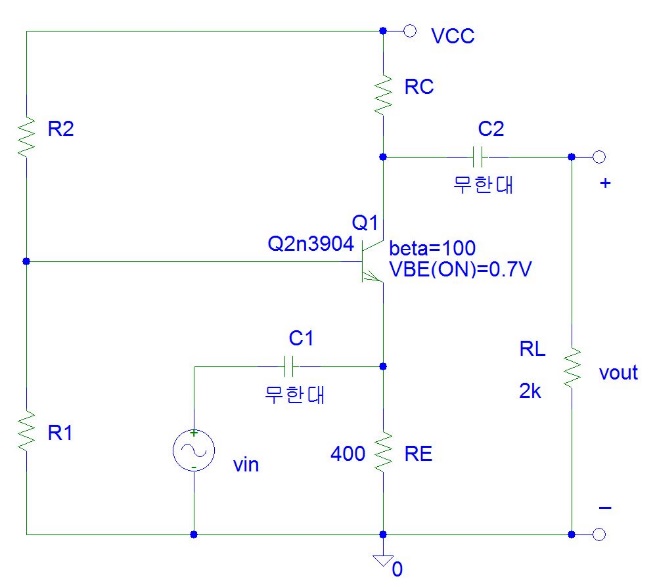
The voltage gain of the CC amplifier is approximately unity. The input resistance is found

*Rin=RB∥[β(RE∥RL)] = 1 kΩ*

The output resistance is found

The maximum peak-to-peak symmetrical output swing is given by

**Analysis of CB Amplifier**



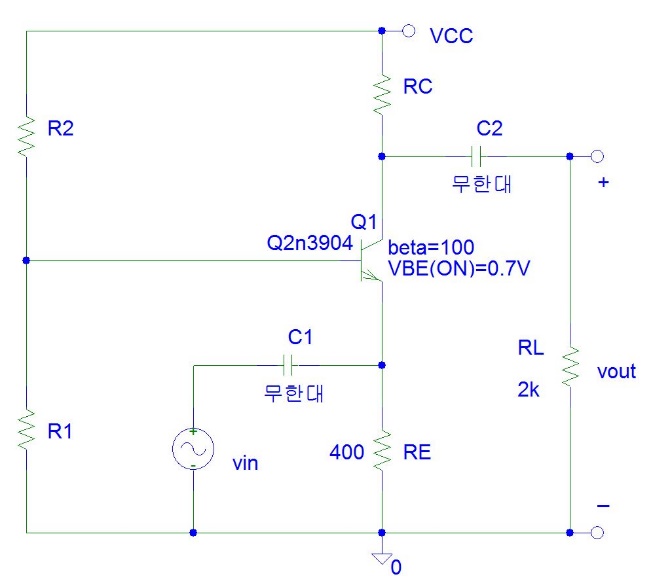
Input resistance ;

Current gain ;

Voltage gain ;

**Design of Capacitor-Coupled CB Amplifier**

Design a CE amplifier using npn transistor with with β=100, VCC=24 V, RL=2 kΩ, RE=400 Ω, and VBE=0.7 V. Design this amplifier for a voltage gain of 20. Verify your design using a computer simulation.



SOLUTION :

We shall choose RC = RL = 2 kΩ

Using the equation for Av, we have

We find Rac and Rdc.

*Rac = RE + (RC∥RL) = 1400 Ω*

*Rdc = RE + RC = 2400 Ω*

With Rac and Rdc determined, the next step is to calculate the quiescent current needed to place the Q-point in the center of the ac load line. The equation is

re is much less than RE, so

We use bias equation to find the parameters of the input bias circuitry.

The bias resistors are then given by

Therefore, we can calculate the input resistance and the current gain

.

The maximum peak-to-peak output swing is given by

**Frequency Responses of Amplifier**

**Time Constant**

All Electrical or Electronic circuits or systems suffer from some form of “time-delay” between its input and output, when a signal or voltage, either continuous, ( DC ) or alternating ( AC ) is firstly applied to it.

This delay is generally known as the **time delay** or **Time Constant** of the circuit and it is the time response of the circuit when a step voltage or signal is firstly applied. The resultant time constant of any electronic circuit or system will mainly depend upon the reactive components either capacitive or inductive connected to it and is a measurement of the response time with units of, (  )

When an increasing DC voltage is applied to a discharged [Capacitor](http://www.electronics-tutorials.ws/capacitor/cap_1.html), the capacitor draws a charging current and “charges up”, and when the voltage is reduced, the capacitor discharges in the opposite direction. Because capacitors are able to store electrical energy they act like small batteries and can store or release the energy as required.

The charge on the plates of the capacitor is given as: Q = CV. This charging (storage) and discharging (release) of a capacitors energy is never instant but takes a certain amount of time to occur with the time taken for the capacitor to charge or discharge to within a certain percentage of its maximum supply value being known as its **Time Constant** (  ).

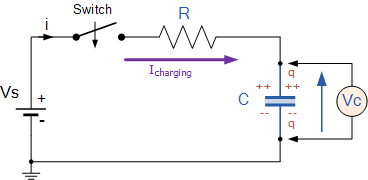
If a resistor is connected in series with the capacitor forming an RC circuit, the capacitor will charge up gradually through the resistor until the voltage across the capacitor reaches that of the supply voltage. The time also called the transient response, required for the capacitor to fully charge is equivalent to about **5 time constants** or 5 .

This transient response time   , is measured in terms of    = R x C, in seconds, where R is the value of the resistor in ohms and C is the value of the capacitor in Farads. This then forms the basis of an RC charging circuit were 5 can also be thought of as “5 x RC”.

**RC Charging Circuit**

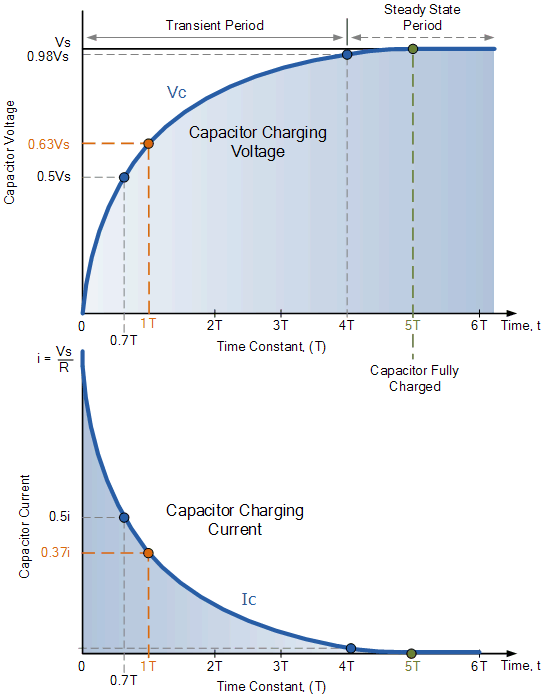
The figure below shows a capacitor, ( C ) in series with a resistor, ( R ) forming a **RC Charging Circuit** connected across a DC battery supply ( Vs ) via a mechanical switch. When the switch is closed, the capacitor will gradually charge up through the resistor until the voltage across it reaches the supply voltage of the battery. The manner in which the capacitor charges up is also shown below.

RC Charging Circuit



Let us assume above, that the capacitor, C is fully “discharged” and the switch (S) is fully open. These are the initial conditions of the circuit, then t = 0, i = 0 and q = 0. When the switch is closed the time begins at t = 0 and current begins to flow into the capacitor via the resistor.

**RC Charging Circuit Curves**



The capacitor now starts to charge up as shown, with the rise in the RC charging curve steeper at the beginning because the charging rate is fastest at the start and then tapers off as the capacitor takes on additional charge at a slower rate.

As the capacitor charges up, the potential difference across its plates slowly increases with the actual time taken for the charge on the capacitor to reach 63% of its maximum possible voltage, in our curve 0.63Vs being known as one Time Constant, (  ).

This 0.63Vs voltage point is given the abbreviation of 1, (one time constant).

The capacitor continues charging up and the voltage difference between Vs and Vc reduces, so to does the circuit current, i. Then at its final condition greater than five time constants (  ) when the capacitor is said to be fully charged, *t = ∞, i = 0, q = Q = CV*. Then at infinity the current diminishes to zero, the capacitor acts like an open circuit condition therefore, the voltage drop is entirely across the capacitor.

So mathematically we can say that the time required for a capacitor to charge up to one time constant, (  ) is given as:

**RC Time Constant,**

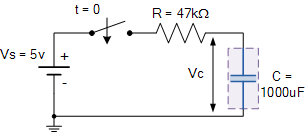
This RC time constant only specifies a rate of charge where, R is in Ω‘s and C in Farads.

After a time of 5 the capacitor is now fully charged and the voltage across the capacitor, ( Vc ) is equal to the supply voltage, ( Vs ). As the capacitor is fully charged no more current flows in the circuit. The time period after this 5 point is known as the **Steady State Period**.

Note that as the charging curve for a RC charging circuit is exponential, the capacitor in reality never becomes 100% fully charged due to the energy stored in the capacitor. So for all practical purposes, after five time constants a capacitor is considered to be fully charged.

**RC Charging Circuit Example No1**

Calculate the RC time constant, τ of the following circuit.

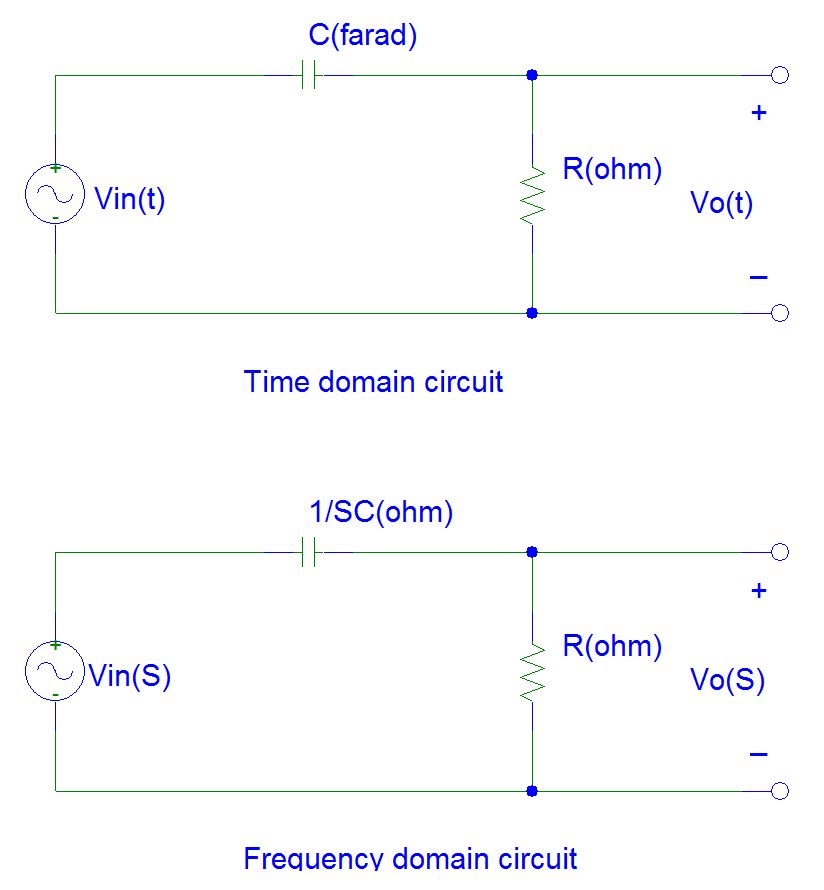


The time constant,   is found using the formula   = R x C in seconds.

Therefore the time constant τ is given as:    = R x C = 47k x 1000uF = 47 secs

**Cutoff Frequency vs Time Constant**

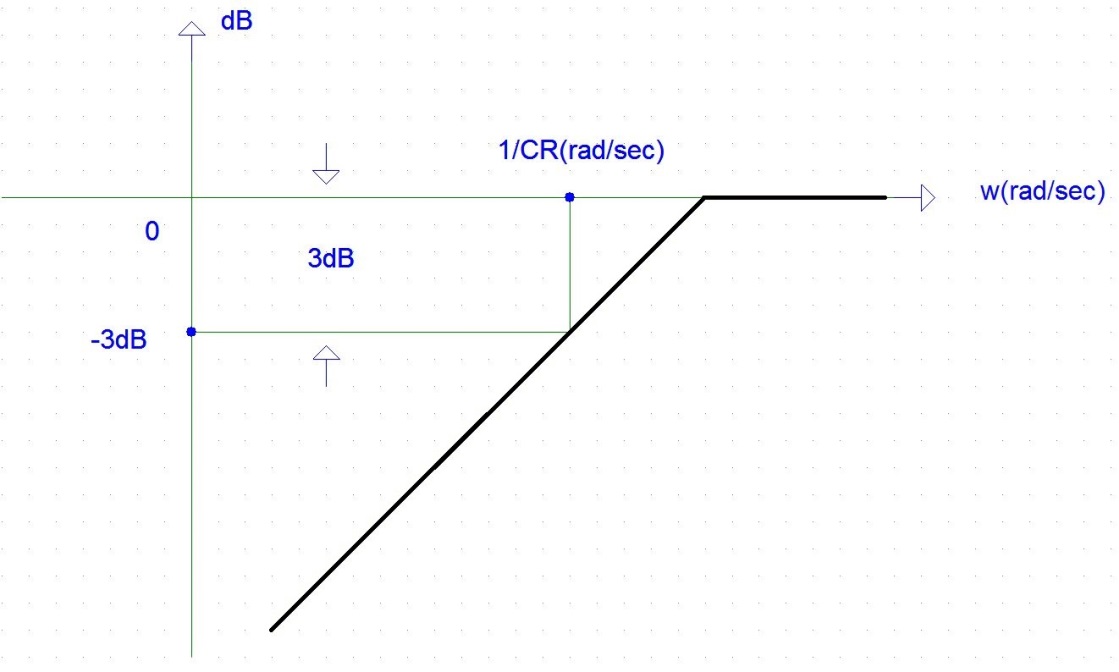
**⒜ 1st order Simple CR Circuit**



The transfer function in frequency domain is

Magnitude response with respect to ω is

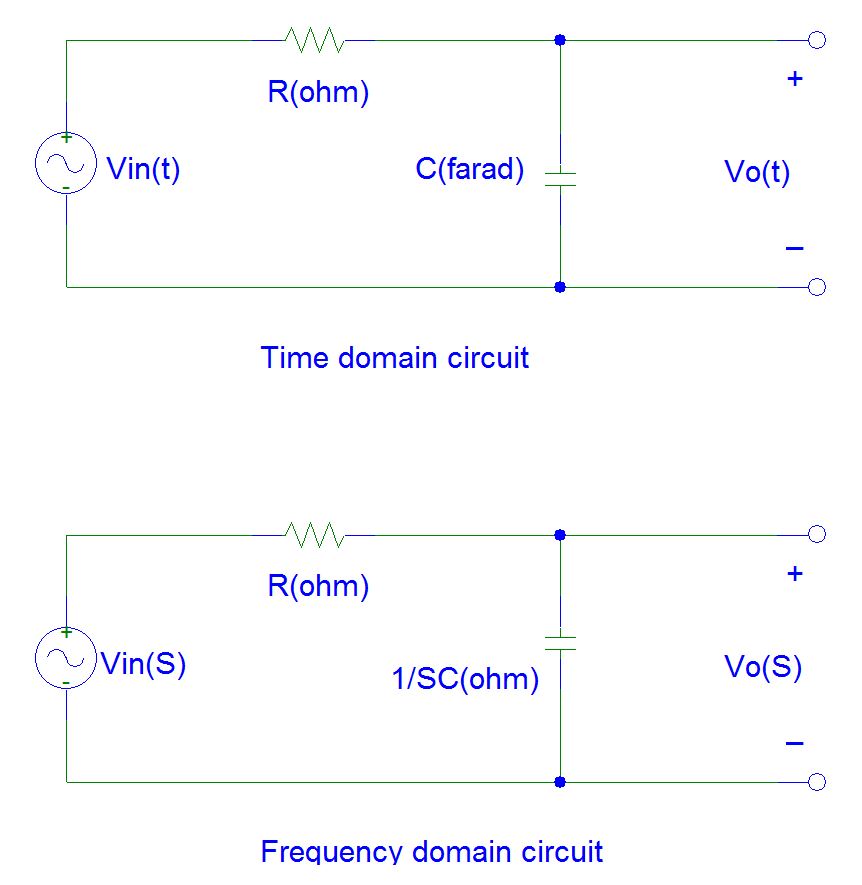
If the frequency of input signal approaches to 0, the gain of the transfer function reaches -∞ dB. While the gain of the transfer function reaches 0 dB. When the input signal frequency is 1/RC (rad/sec), the magnitude of H(S) is i.e. -3 dB.



Therefore, the cutoff frequency of the simple C-R circuit is

***This means that the cutoff frequency is equal to the reciprocal of the time constant of the capacitor in the CR first order circuit.***

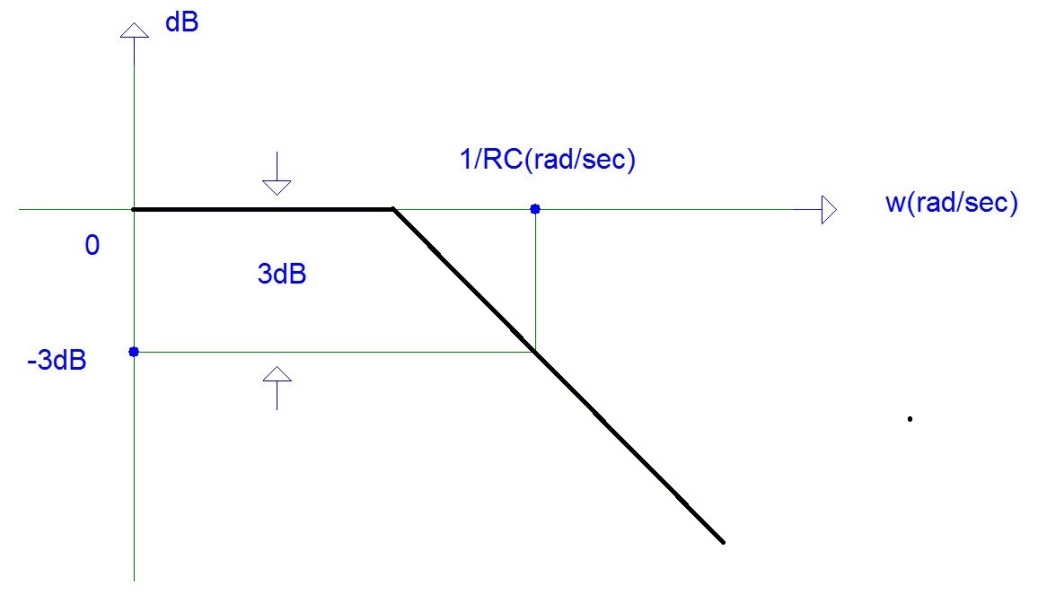
**⒝** **1st order Simple RC Circuit**



The transfer function in frequency domain is

Magnitude response with respect to ω is

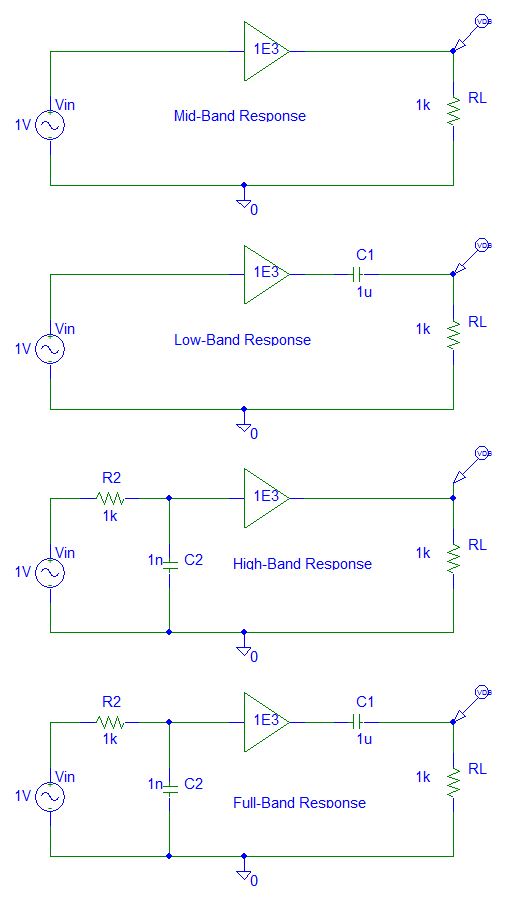
If the frequency of input signal approaches to 0, the gain of the transfer function reaches 0 dB. While the gain of the transfer function reaches -∞dB when the frequency of the input signal reaches ∞. When the input signal frequency is 1/RC (rad/sec), the magnitude of H(S) is i.e. -3 dB.



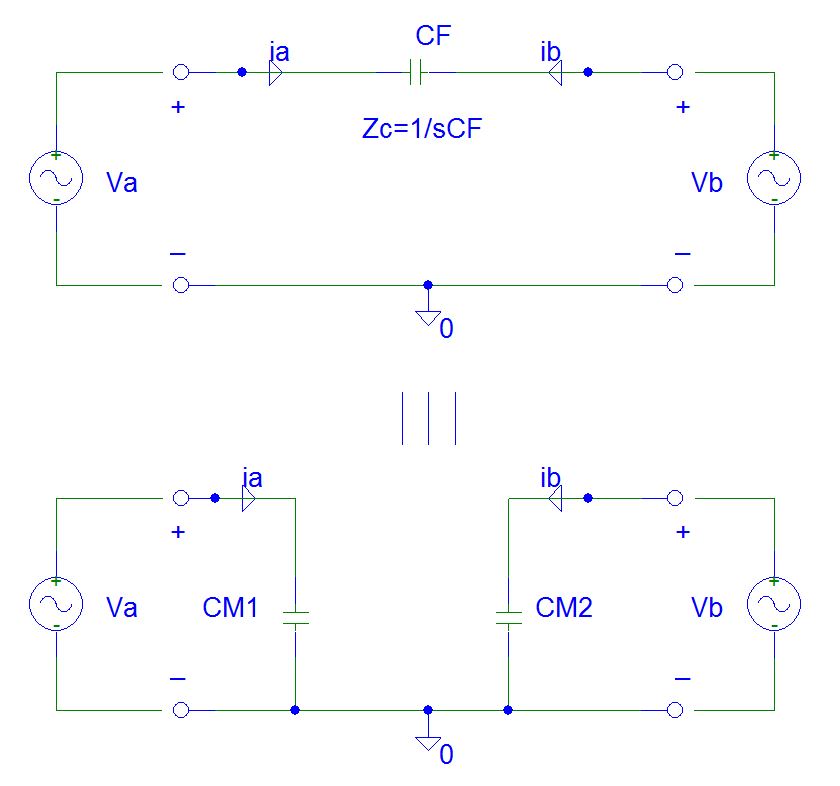
Therefore, the cutoff frequency of the simple R-C circuit is

***This means that the cutoff frequency is equal to the reciprocal of the time constant of the capacitor in the RC first order circuit.***

**(Example 1) Bandwidth Design**

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**⒞ Miller Effect (Miller Capacitor)**

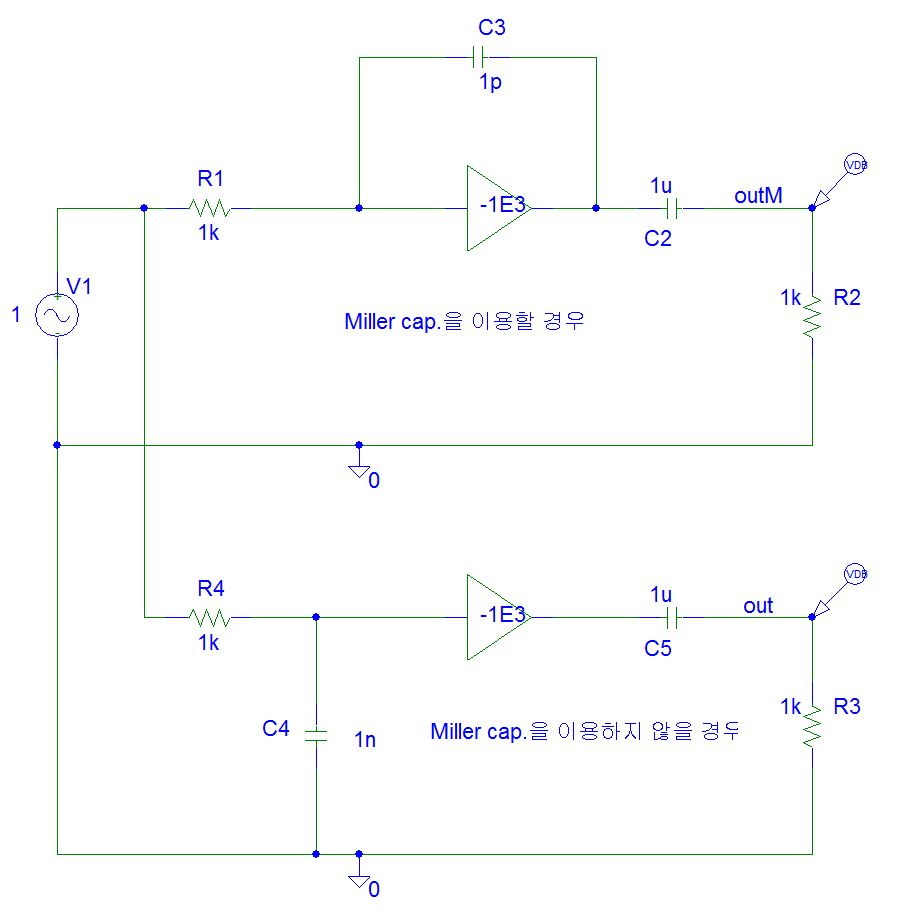


At the input terminal, the relationship between voltage *va* and current *ia*is

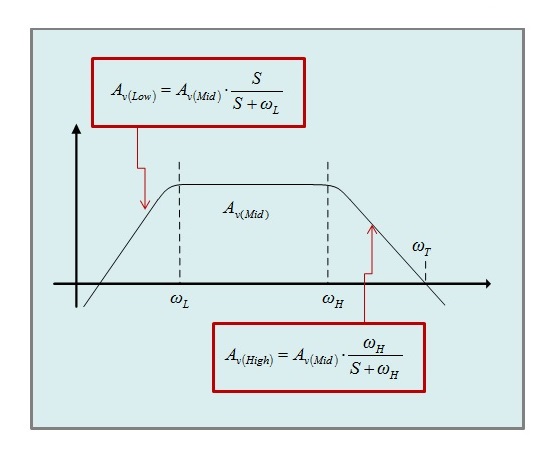
At the input terminal, the relationship between voltage *vb* and current *ib*is

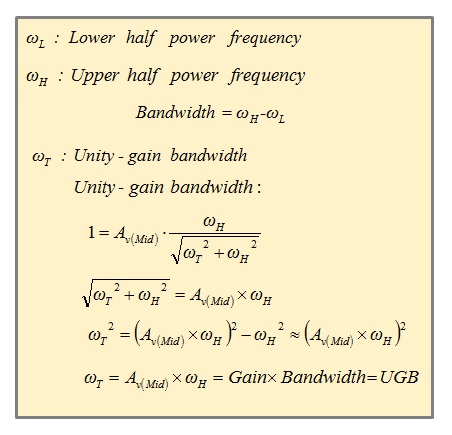
If *Avi* is much larger than 1 and is out of phase, *CM1* and *CM2* are approximately

**(Example 2) Miller capacitor**



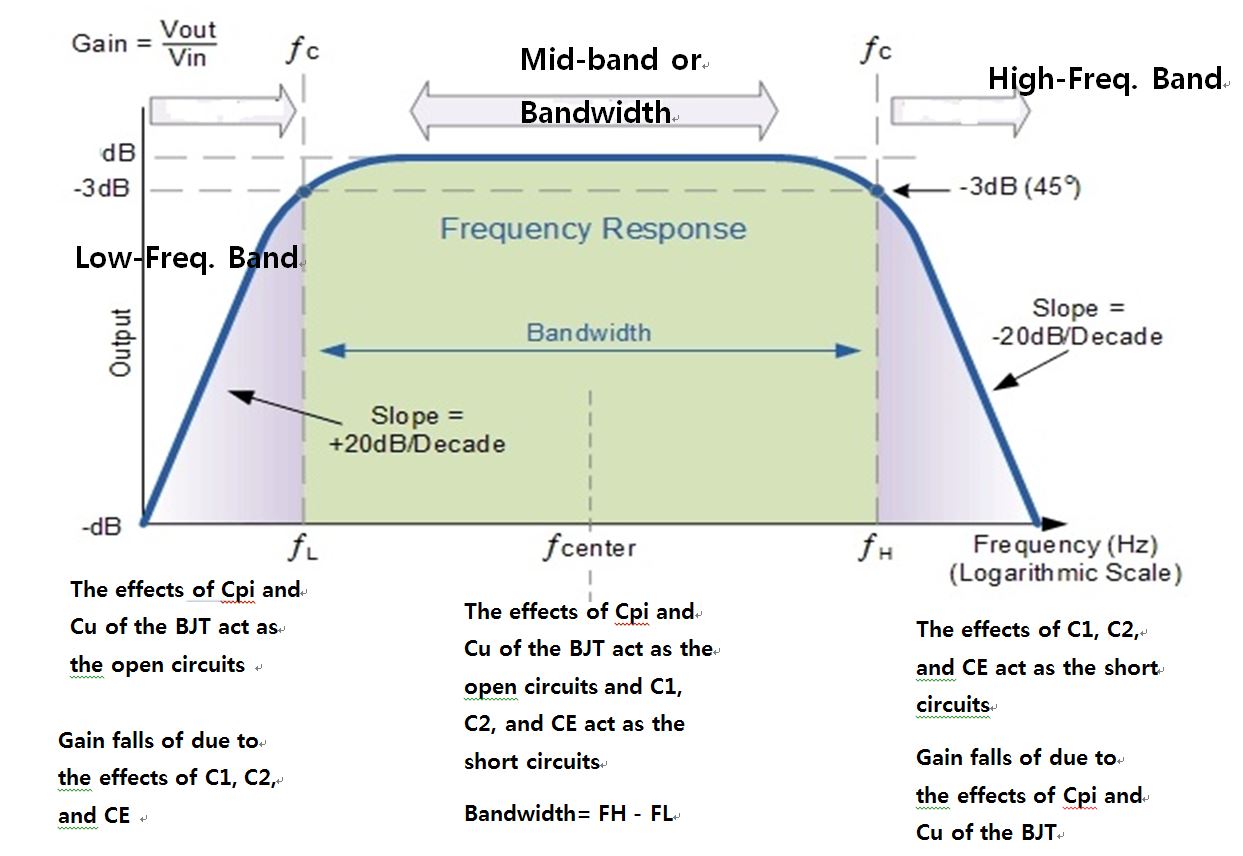
**(Example 3) Total Frequency Response of Amplifier**





**AC circuit of CE amplifier**



****

**Mid-Frequency Response of CE Amplifier**

Capacitor *C1*, *C2*, and *CE* act as short circuit.

Capacitor *CF* acts as open circuit.



**Low-Frequency Response of CE Amplifier**

A BJT amplifier is shown in Figure 1. Each circuit has its own cutoff frequency, which is calculated using the relationship shown. Note that the lower cutoff frequencies for the base , collector , and emitter , circuits are calculated. The *highest* cutoff frequency calculated is the overall value of, for the circuit.

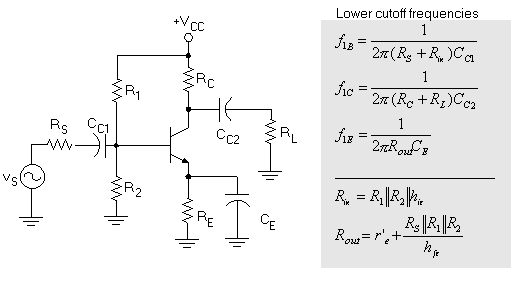


Figure 1 BJT amplifier lower cutoff frequencies

Capacitor *CF* acts as open circuit. The small signal equivalent circuit in low frequency range is

Lower frequency due to *CC1* is



Lower frequency due to *CC2* is



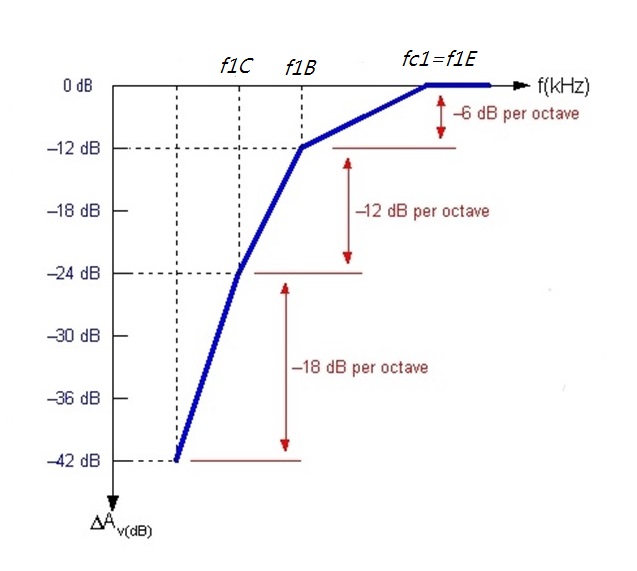
Lower frequency due to *CE* is



Among the lower cutoff frequencies for the base , collector , and emitter , one of them sets to be lower half frequency . Rest of them must set to be smaller than lower half frequency.

For example, if sets to be , then

or



**High-Frequency Response of CE Amplifier**

The high-frequency equivalent of a BJT amplifier is shown in Figure 2 with *C1*, *C2*, and *CE* act as short circuit. Each circuit has its own cutoff frequency, which is calculated using the relationship shown. Note that the upper cutoff frequencies for the base , and collector , circuits are calculated, and the *lowest* result is the overall value of , for the circuit.

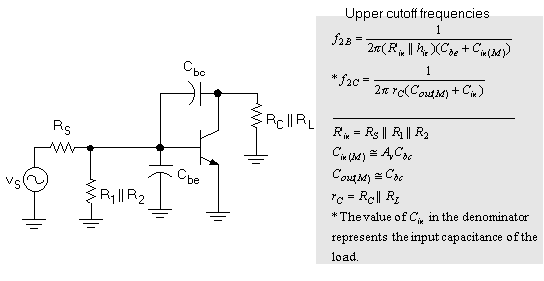


Figure 2 BJT amplifier upper cutoff frequencies.

The small signal equivalent circuit in high frequency range is



The equations in Figure 2 contain the variables and . These variables represent the **Miller capacitance** values for the circuit. Miller’s theorem states that a feedback capacitor (such as ) can be represented as separate input and output capacitance values (which simplifies the analysis of the circuit). The values of the Miller capacitances are found using the relationships shown in the figure.

Using Miller effect, modify the equivalent circuit.



Upper 3dB frequency due to *CM1* is



Upper 3dB frequency due to *CM2* is



Generally the upper half power frequency is determined by *CM1* because the value of *CM1* is much larger than that of *CM2*.

Therefore,